REMARKS

Claims 1-26 are pending in the present patent application. Claims 12-23 stand rejected. Claims 1-11 and 24-26 have been withdrawn from consideration. By this amendment, claim 22 has been amended. This application continues to include claims 1-26.

Applicants note that the present Office Action does not indicate whether the drawings were accepted by the Examiner. Applicants respectfully request the Examiner to indicate whether the drawings have been accepted.

Claims 12 and 14-23 were rejected under 35 U.S.C. §103(a) as being unpatentable over Carpenter, Jr., et al., U.S. Patent No. 6,469,884 B1 (hereinafter, Carpenter) in view of Yamazaki, U.S. Patent No. 5,180,967 (hereinafter, Yamazaki). Applicants respectfully request reconsideration of the rejection of claims 12 and 14-23 in view of the following.

Carpenter is directed to internal ESD protection circuits for on chip programmable polysilicon fuses (col. 1, lines 11-12). Carpenter discloses a polysilicon fuse F1 coupled between a main voltage supply potential V_{main} and a programming MOSFET switch MN_{main} coupled between the fuse F1 and ground, which is adapted to conduct current and selectively blow the polysilicon fuse F1 upon a logic high being provided to the gate of the enable switch MN_{main} (col. 3, lines 49-55, Fig. 1). A MOSFET MN_{read} coupled between the polysilicon fuse F1 and a Schmitt fuse detector 12 being powered by a voltage potential V_{cc} (col. 4, lines 63-66).

Yamazaki is directed to a self-activated constant-current source circuit (col. 1, lines 10-11). Yamazaki discloses an embodiment of a constant-current source circuit 200 having a first current mirror circuit 202, a second current mirror circuit 208, a resistor 214, a fifth NMOS transistor 216, a sixth NMOS transistor 218 and a seventh PMOS transistor 220 (col. 7, lines 35-39). The first current mirror circuit 202 has first and second PMOS transistors 204 and 206,

whereas the second current mirror circuit 208 has third and fourth NMOS transistors, 210 and 212 (col. 7, lines 40-43).

Applicants believe that claims 12 and 14-23 patentably define Applicants' invention over Carpenter and Yamazaki, taken alone or in combination, for at least the reasons set forth below.

Claim 12 is directed to a sense circuit for reading a fusible link. Claim 12 recites a first transistor defining a read input for receiving a read signal, a first terminal coupled to said fusible link, and a second terminal coupled to an output port; and a second transistor having a bias input biased to a voltage reference, having a third terminal coupled to said second terminal of said first transistor, and a fourth terminal coupled to a ground.

Carpenter does not disclose, teach, or suggest a second transistor having a bias input biased to a voltage reference, having a third terminal coupled to the second terminal of the first transistor, and a fourth terminal coupled to a ground, nor does the Examiner assert as much.

Rather, Yamazaki is relied on as assertedly disclosing a second transistor having a bias input biased to a voltage reference, having a third terminal coupled to the second terminal of the first transistor, and a fourth terminal coupled to a ground.

In particular, the Yamazaki transistor 216 is asserted to be the second transistor of claim 12.

However, in contrast to the second transistor of claim 12, which has a bias input biased to a voltage reference, the Yamazaki transistor 216 is coupled to a first current mirror circuit 202 and a second current mirror circuit 208. The first current mirror circuit 202 has a terminal coupled to a resistor 214 that is itself coupled to a voltage V_{DD}, and the second current mirror circuit 208 is coupled to the first current mirror circuit 202 at one terminal, and coupled to ground at the other terminal.

Thus, in contrast to a bias input biased to a voltage reference, the Yamazaki transistor 216 bias input is coupled between two current mirror circuits that are downstream of a resistor that is coupled to voltage V_{DD}. Because the transistor 216 is coupled to first current mirror circuit 202 and second current mirror circuit 208, the voltage supplied to transistor 216 depends on the state of the first and second current mirrors, and hence is not a reference voltage within the context of Applicants' specification and claims.

For example, as depicted in Applicants' Fig. 3, transistor M1 is biased to voltage reference ppwr without any components in between as might alter the reference voltage supplied at ppwr, unlike Yamazaki transistor 216.

Accordingly, Yamazaki does not disclose, teach, or suggest a second transistor having a bias input biased to a voltage reference, having a third terminal coupled to the second terminal of the first transistor, and a fourth terminal coupled to a ground.

Notwithstanding the above, Applicants respectfully submit that it would not be obvious to combine Yamazaki with Carpenter in an attempt to yield Applicants' invention of claim 12.

For example, MPEP 2144 provides that the expectation of some advantage is the strongest rationale for combining references.

In particular, MPEP 2144 provides that the strongest rationale for combining references is a recognition, expressly or impliedly in the prior art or drawn from a convincing line of reasoning based on established scientific principles or legal precedent, that some advantage or expected beneficial result would have been produced by their combination. *In re Sernaker*, 702 F.2d 989, 994-95, 217 USPQ 1, 5-6 (Fed. Cir. 1983).

However, there is no recognition, expressly or impliedly in the prior art or drawn from a convincing line of reasoning based on established scientific principles or legal precedent, that

some advantage or expected beneficial result would have been produced by combining Yamazaki with Carpenter, nor has the Examiner asserted what such an advantage would be.

Rather, it is asserted that it would be obvious to one having ordinary skill in the art to use Yamazaki's current source in place of Carpenter's current source to provide a constant current source to the circuit, without any explanation or convincing line of reasoning based on established scientific principles or legal precedent, that some advantage or expected beneficial result would be produced.

In addition, MPEP 2143.01(V) provides that if proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification.

However, Carpenter indicates that devices that provide a relatively constant pull down current reduce the speed of switches used to blow the fuse, and often cannot discharge the gate of MOSFETS fast enough during a transient to the operating voltage supply, which allows possible damage to the fuse or accidentally blows the fuse, rendering the integrated circuit in an unintentional or inoperable circuit configuration.

For example, Carpenter discloses at column 1, lines 41-55, as follows:

> One known solution uses long channel MOSFET devices providing a relatively constant pull down current to programming switch devices. The long channel MOSFET is added from switches gate to ground. However, these devices pull-down voltages to operating circuitry all the time, whereby this constant pull-down voltages reduces the speed at which switches used to blow the polysilicon fuses is reduced. Moreover, these pull-down circuits often can not discharge the gate of MOSFETS fast enough during a transient to the operating voltage supply, which consequently allows possible damaging the polysilicon fuses or accidently [sic] blowing the fuses, and perhaps rendering the integrated circuit in an unintentional or inoperable circuit configuration. (Emphasis added).

Thus, the teachings of Carpenter militate against the combination, since, based on the teachings of Carpenter, there may be adverse effects associated with combining the constant current source of Yamazaki with the Carpenter circuit, and hence, it would not be obvious to combine Yamazaki with Carpenter in an attempt to yield Applicants' invention of claim 12.

Further, MPEP 2143.02 provides that the prior art can be modified or combined to reject claims as prima facie obvious as long as there is a reasonable expectation of success. *In re Merck & Co., Inc.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

However, it has not been shown that the combination of the Yamazaki constant current source with the Carpenter circuit would yield a reasonable expectation of success. In addition, the teachings of Carpenter, reproduced above, militate against a reasonable expectation of success of the asserted combination.

Still further, MPEP 2143.01 provides that the prior art must suggest the desirability of the claimed invention. However, there is nothing in either Carpenter or Yamazaki that suggests the desirability of combining Carpenter and Yamazaki to realize the invention of claim 12.

Accordingly for at least the reasons set forth above, it would not be obvious to combine Yamazaki with Carpenter, and even if combined, the resultant combination would not yield Applicants' invention of claim 12.

Claim 12 is thus believed allowable in its present form.

Claims 14-23 are believed allowable due to their dependence, directly or indirectly, on otherwise allowable base claim 12. In addition, claims 14-23 further and patentably define the invention over Carpenter and Yamazaki, taken alone or in combination.

For example, claim 14 is directed to the sense circuit of claim 12, wherein an output voltage at said output port in a range of about 1 volt to about 2.5 volts signifies that said fusible link is opened.

Carpenter and Yamazaki, taken alone or in combination, do not disclose, teach, or suggest wherein an output voltage at said output port in a range of about 1 volt to about 2.5 volts signifies that the fusible link is opened, as recited in claim 14, nor does the Examiner assert as much.

Rather, the Examiner asserts that the value is ascertainable by routine experimentation, that optimization of range limitations are prima facie obvious, and that it would be obvious to select the output voltage value or the opened fuse resistance value dependent upon the particular environment of use to ensure optimum performance.

However, MPEP 2144.05(II)(B) provides that only result-effective variables can be optimized.

In particular, MPEP 2144.05(II)B) sets forth that a particular parameter must first be recognized as a result-effective variable, i.e., a variable which achieves a recognized result, before the determination of the optimum or workable ranges of said variable might be characterized as routine experimentation. *In re Antonie*, 559 F.2d 618, 195 USPQ 6 (CCPA 1977).

Regarding *In re Antonie*, the prior art did not recognize that treatment capacity is a function of the tank volume to contractor ratio, and therefore the parameter optimized was not recognized in the art to be a result-effective variable. (MPEP 2144.05(II)(B).

Applicants respectfully submit that neither Carpenter nor Yamazaki disclose, teach, or suggest a recognition that an output voltage at the output port in a particular nonzero voltage or range of voltages signifies that the fusible link is opened, and hence, the parameter is not recognized in the art to be a result-effective variable.

For example, although Carpenter discloses that if the fuse F1 is blown, a 0 voltage potential at node D will be provided to input V_{in} and detectable at output node E, this does not disclose, teach, or suggest a recognition that an output voltage at the output port in a particular nonzero range signifies that the fusible link is opened.

Yamazaki does not disclose, teach, or suggest anything about fuses, and hence, does not disclose, teach, or suggest a recognition that an output voltage at the output port in a particular nonzero range signifies that the fusible link is opened.

Accordingly, the parameter is not recognized in the art to be a result-effective variable, and hence, under MPEP 2144.05(II)B), claim 14 is not obvious over Carpenter and Yamakazi, taken alone or in combination.

Claim 14 is thus believed allowable in its own right.

Claim 15 is directed to the sense circuit of claim 12, wherein an output voltage at said output port of about 1.5 volts signifies that said fusible link is opened.

Claim 15 is believed allowable in its own right for substantially the same reasons as set forth above with respect to claim 14.

Claim 16 is directed to the sense circuit of claim 12, wherein an output voltage at said output port indicates that said fusible link is opened when said fusible link has a resistance in a range of about 1k ohms to about 2k ohms.

Carpenter and Yamazaki, taken alone or in combination, do not disclose, teach, or suggest wherein an output voltage at said output port indicates that said fusible link is opened when said fusible link has a resistance in a range of about 1k ohms to about 2k ohms, as recited in claim 16, nor does the Examiner assert as much.

Rather, the Examiner asserts that the value is ascertainable by routine experimentation, that optimization of range limitations are prima facie obvious, and that it would be obvious to select the output voltage value or the opened fuse resistance value dependent upon the particular environment of use to ensure optimum performance.

However, MPEP 2144.05(II)(B) provides that only result-effective variables can be optimized.

In particular, MPEP 2144.05(II)B) sets forth that a particular parameter must first be recognized as a result-effective variable, i.e., a variable which achieves a recognized result, before the determination of the optimum or workable ranges of said variable might be characterized as routine experimentation. *In re Antonie*, 559 F.2d 618, 195 USPQ 6 (CCPA 1977).

Regarding *In re Antonie*, the prior art did not recognize that treatment capacity is a function of the tank volume to contractor ratio, and therefore the parameter optimized was not recognized in the art to be a result- effective variable. (MPEP 2144.05(II)(B).

Applicants respectfully submit that neither Carpenter nor Yamazaki disclose, teach, or suggest a recognition that a fusible link has a particular resistance or range of resistance values that indicate that the fusible link is opened, and hence, the parameter is not recognized in the art to be a result-effective variable.

For example, although Carpenter discloses that if the fuse F1 is blown, a 0 voltage potential at node D will be provided to input V_{in} and detectable at output node E, this does not disclose, teach, or suggest a recognition that a fusible link has a particular resistance or range of resistance values that indicate that the fusible link is opened.

Yamazaki does not disclose, teach, or suggest anything about fuses, and hence, does not disclose, teach, or suggest a recognition that a fusible link has a particular resistance or range of resistance values that indicate that the fusible link is opened.

Accordingly, the parameter is not recognized in the art to be a result-effective variable, and hence, under MPEP 2144.05(II)B), claim 16 is not obvious over Carpenter and Yamakazi, taken alone or in combination.

Claim 16 is thus believed allowable in its own right.

Claims 17-21 are believed allowable in their own respective rights for substantially the same reasons as set forth above with respect to claim 16.

Claim 22 is directed to the sense circuit of claim 12, and as amended, recites a third transistor having a bias input biased to said voltage reference, having a fifth terminal coupled between said fusible link and said first terminal of said first transistor, and having a sixth terminal coupled to ground.

Thus, the third transistor of claim 22 has a bias input biased to the same voltage reference as the bias input of the second transistor.

In contrast, the Carpenter MN_{main} and MN_{read} transistors are not biased to the same voltage.

In addition, the Yamazaki transistor 216 is not biased to the voltage reference for substantially the same reasons as set forth above with respect to claim 12.

Further, it would not be obvious to combine Yamakazi with Carpenter for substantially the same reasons as set forth above with respect to claim 12.

Accordingly, claim 22 is believed allowable in its own right.

Claim 23 is directed to the sense circuit of claim 12, said sense circuit being incorporated in at least one of an ink jet printhead and an ink jet printer.

Carpenter and Yamakazi, taken alone or in combination, do not disclose, teach, or suggest a sense circuit being incorporated in at least one of an ink jet printhead and an ink jet printer, nor does the Examiner assert as much.

Rather, the Examiner asserts that it is known in the art that an ink jet printhead and an ink jet printer have a fuse sense circuit.

However, to establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. MPEP 2143 (Emphasis added).

Since Carpenter and Yamakazi, taken alone or in combination, do not disclose, teach, or suggest an ink jet printhead or ink jet printer, much less the sense circuit being incorporated in at least one of an ink jet printhead and an ink jet printer, a prima facie case of obviousness has not been established as against claim 23 under MPEP 2143.

Accordingly, claim 23 is believed allowable in its own right.

Accordingly, for at least the reasons set forth above, Applicants believe that claims 12 and 14-23 are in condition for allowance in their present form, and thus respectfully request that the rejection of claims 12 and 14-23 under 35 U.S.C. 103(a) be withdrawn

Claim 13 was rejected under 35 U.S.C. §103(a) as being unpatentable over Carpenter in view of Yamazaki and Erstad, U.S. Patent No. 6,833,749 B2 (hereinafter, Erstad). Applicants respectfully request reconsideration of the rejection of claim 13 in view of the following.

Erstad is directed to generating hysteresis in a digital circuit (col. 1, lines 8-9). Erstad discloses a second inverter 240 that inverts a signal at an inner signal node 226 received from a first inverter 230, producing a signal at an OUT1 terminal 204 (col. 3, lines 62-65).

Applicants believe that claim 13 patentably defines Applicants' invention over Carpenter, Yamazaki, and Erstad, taken alone or in combination, for at least the reasons set forth below.

Claim 13 is directed to the sense circuit of claim 12, further comprising an inverter circuit coupled between said second terminal of said first transistor and said output port.

Carpenter and Yamazaki, taken alone or in combination, do not disclose, teach, or suggest an inverter circuit coupled between the second terminal of the first transistor and the output port, nor does the Examiner assert as much.

Rather, Erstad is relied upon as disclosing an inverter. In particular, it is asserted that it would be obvious to use the Erstad inverter 230 for Carpenter's Schmitt trigger for the purpose of reducing noise.

However, the inverter would invert the signal otherwise output by Carpenter's Schmitt trigger, hence inverting the output of the Carpenter circuit.

If proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. *In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984) (MPEP 2143.01(V)).

Since the Erstad inverter 230 would invert the signal otherwise output by Carpenter's Schmitt trigger, hence inverting the output of the Carpenter circuit, the modification of Carpenter with Erstad would render the Carpenter circuit unsatisfactory for its intended purpose, and hence, under MPEP 2143.01(V), there would be no motivation to modify Carpenter with Erstad.

In addition, it would not be obvious to combine Yamakazi with Carpenter for substantially the same reasons as set forth above with respect to claim 12.

Accordingly, claim 13 is not unpatentable as being obvious over Carpenter in view of Yamakazi and Erstad.

In addition, claim 13 is believed allowable due to its dependence on otherwise allowable base claim 12.

Accordingly, for at least the reasons set forth above, Applicants believe that claim 13 is in condition for allowance in its present form, and thus respectfully request that the rejection of claim 13 under 35 U.S.C. 103(a) be withdrawn.

For the foregoing reasons, Applicants submit that no combination of the cited references teaches, discloses or suggests the subject matter of the appended claims, and that the appended claims are not obvious in view of the cited references. The appended claims are therefore in condition for allowance, and Applicants respectfully request withdrawal of all rejections and allowance of the claims.

In the event Applicants have overlooked the need for an extension of time, an additional extension of time, payment of fee, or additional payment of fee, Applicants hereby conditionally petition therefor and authorize that any charges be made to Deposit Account No. 20-0095, TAYLOR & AUST, P.C.

Should any question concerning any of the foregoing arise, the Examiner is invited to telephone the undersigned at (317) 894-0801.

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